ABSTRACT OF THE DISCLOSURE

A level transforming circuit includes a first CMOS circuit, a first intermediate circuit, a second intermediate circuit, a second CMOS circuit, a seventh p-channel type MOS transistor, and an eighth p-channel type MOS transistor; wherein the first intermediate circuit and the second intermediate circuit form a latch circuit. To this latch circuit, writing of data is performed by way of the seventh p-channel type MOS transistor and the eighth p-channel type MOS transistor. Thus, the latch circuit is made up of a CMOS inverter. Therefore, fast operation can be obtained and drop of drivability can be restrained.